IN THE CLAIMS:

Please amend the claims to read as follows:

Claims 1-4 (Canceled).

Claim 5 (Currently Amended) A method for supplying a power to a liquid crystal display, comprising the steps of:

taking a power source voltage less than 3.0V from a system; [[and]]

supplying the power source voltage less than 3.0V to ~~digital circuit devices including~~ an interface circuit, a timing controller, a data driving circuit and a gate driving circuit for processing digital signal ~~with respect to a reference voltage provided from a DC-DC converter;~~ and

raising or reducing the power source voltage less than 3.0V using a DC-DC converter to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL, wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit.

Claims 6 – 17 (Canceled)

Claim 18 (Currently Amended) An apparatus for supplying a power to a liquid crystal display comprising:

a system for generating a power source voltage under 3.0V; [[and]]

~~digital circuit devices including~~ an interface circuit, a timing controller, a data driving circuit and a gate driving circuit used to process the digital signal ~~with respect to a reference voltage provided from a DC-DC converter~~ by taking the power source voltage; and

a DC-DC converter for raising or reducing the power source voltage under 3.0V to generate a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL, wherein the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 are supplied to the data driving circuit, and the gate high voltage VGH and the gate low voltage VGL are supplied to the gate driving circuit,

wherein the power source voltage is supplied to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit.

Claim 19 (Canceled)

Claim 20 (Currently Amended) The apparatus for supplying a power to [[of]] a liquid crystal display according to claim 18, wherein ~~the digital circuit devices further include:~~

[[an]] the interface circuit ~~for receiving~~ receives a synchronous signal, a clock signal and digital video data from the system; and

[[a]] the timing controller ~~for controlling~~ controls the data driving circuit and the gate driving circuit by using the synchronous signal and the clock signal from the interface circuit,

wherein the data driving circuit supplies the digital video data to the liquid crystal panel and the gate driving circuit supplies a scan pulse to the liquid crystal panel.

Claim 21 (Canceled).

Claim 22 (Currently Amended) A method for supplying a power to a liquid crystal display, having ~~digital circuit devices including~~ an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is ~~over 3.0V~~ 3.3V;

generating a second power source voltage less than 3.0V from the first power source voltage of 3.3V using a reducing circuit[[,]] ;

supplying the second power source voltage less than 3.0V to the interface circuit, the timing controller, the data driving circuit, and the gate driving circuit for processing ~~being used to process~~ digital signal of the ~~digital circuit devices and at least lower than the first power source voltage~~ interface circuit, the timing controller, the data driving circuit, and the gate driving circuit;

generating ~~third power source voltages~~ a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter~~, the third power source voltages~~

~~being used as reference voltage of the digital circuit devices~~; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate low voltage to the gate driving voltage ~~the second power source voltage and the third power source voltages to the digital circuit devices~~.

Claim 23 - 26 (Canceled)

Claim 27 (Currently Amended) A method for supplying a power to a liquid crystal display, having ~~digital circuit devices including~~ an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a [[first]] power source voltage from a system wherein the [[first]] power source voltage is ~~at least lower~~ less than 3.0V ~~and is used to process digital signal of the digital circuit devices~~;

supplying the power source voltage to the interface circuit, the timing controller, the data driving circuit and the gate driving circuit;

generating ~~second power source voltages~~ a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the [[first]] power source voltage less than 3.0V using a DC-DC converter~~, the second power source voltages being used as reference voltage of the digital circuit devices~~; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate

low voltage to the gate driving voltage ~~the first power source voltage and the second power source voltages to the digital circuit devices~~.

Claim 28 - 31 (Canceled)

Claim 32 (New) A method for supplying a power to a liquid crystal display, having an interface circuit, a timing controller, a data driving circuit, and a gate driving circuit for processing digital signal, comprising the steps of:

providing a first power source voltage from a system wherein the first power source voltage is 3.3V;

supplying the first power source voltage of 3.0V to the data driving circuit and the gate driving circuit for processing digital signal of the data driving circuit and the gate driving circuit;

generating a second power source voltage less than 3.0V from the first power source voltage of 3.3V using a reducing circuit;

supplying the second power source voltage less than 3.0V to the interface circuit and the timing controller for processing digital signal of the interface circuit and the timing controller;

generating a reference voltage VDD, a common voltage VCOM, gamma voltages GMA1~10, a gate high voltage VGH and a gate low voltage VGL from the first power source voltage of 3.3V using a DC-DC converter; and

supplying the reference voltage VDD, the common voltage VCOM and the gamma voltages GMA1~10 to the data driving circuit and supplying the gate high voltage and the gate

low voltage to the gate driving voltage.